

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	17	703/20.ccls. and @pd>="20080220"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/07/11 18:28
L4	66	soc and verify\$7 and ((test adj bench) or testbench) and @ad<"20020301"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/07/11 18:41



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soc verification testbench

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Scholar All articles - Recent articles Results 1 - 10 of about 312 for **soc verification testbench**. (0.4s)

Nuts and Bolts of Core and SoC Verification - all 14 versions »

K Albin - 38th Design Automation Conference (DAC'01), 2001 - doi.ieeecomputersociety.org

... 3.1.3 the ability to organize large amounts of data **SoC** designs are large ... Monitors

Figure 1 shows the basic components of a unit-level **verification testbench** ...

Cited by 26 - Related Articles - Web Search

book **Surviving the Soc Revolution: A Guide to Platform-Based Design**

H Chang - 1999 - Kluwer Academic Publishers

Cited by 294 - Related Articles - Web Search

book **System-On-A-Chip Verification: Methodology and Techniques** - all 2 versions »

P Rashinkar, P Paterson, L Singh - 2001 - books.google.com

... This anecdote motivates this book on **SOC verification**. Effective verification is fundamental to design reuse ... be accompanied by a reusable "complete" testbench ...

Cited by 106 - Related Articles - Web Search

Verification of configurable processor cores - all 10 versions »

M Puig-Medina, G Ezer, P Konas - Annual ACM IEEE Design Automation Conference: Proceedings of ..., 2000 - doi.ieeecomputersociety.org

... **TESTBENCH** Emulated System Monitors ... the processor RTL, the **verification** suite, and the system **test-bench** ... be easily merged into an **SOC verification** environment. ...

Cited by 18 - Related Articles - Web Search - [BL Direct](#)

[PDF] Practical Approaches to SOC Verification - all 2 versions »

G Mosenoson - Proceedings of DATE User Forum, 2000 - cecs.uci.edu

... effect they have on the design of the **testbench**. The rest of this paper focuses on showing practical and novel approaches to the **verification of SOC** designs. ...

Cited by 8 - Related Articles - View as HTML - Web Search

C-based SoC design flow and EDA tools: an ASIC and system vendor perspective

K Wakabayashi, T Okamoto - Computer-Aided Design of Integrated Circuits and Systems, ..., 2000 - ieeexplore.ieee.org

... and semi-formal verifiers, and **test-bench** generators. The **verification** tools are tightly integrated with the HLS ... feature into the C-based **SoC** design environment ...

Cited by 68 - Related Articles - Web Search - [BL Direct](#)

A framework for object oriented hardware specification, **verification**, and synthesis - all 18 versions »

T Kuhn, T Oppold, M Winterholer, W Rosenstiel, M ... - Proceedings of the Design Automation Conference (DAC'2001), 2001 - doi.ieeecomputersociety.org

... **Test bench** in 'e' eSS ... environment may be subject to synthesis which may facilitate **test bench** acceleration and ... Practical Approaches to **SOC Verification**. ...

Cited by 31 - Related Articles - Web Search

[PDF] SoC Verification Software—Test Operating System

R Devins - IEEE/DATC Electronic Design Processes Workshop, April, 2001 - eda-stds.org

... System **verification** often involves external, or off-chip data ... consider the off-chip